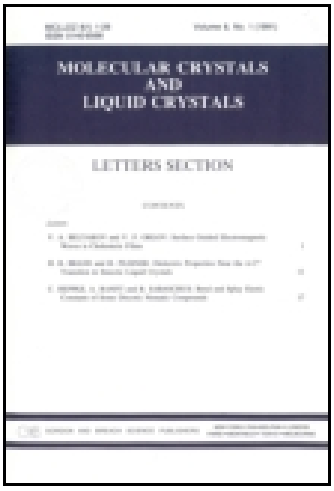

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Ambipolar-Type Organic Field-Effect Transistor with Two Stacked Active Layers in Dual-Gate Configuration

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We demonstrated an ambipolar-type organic field-effect transistor (OFET) in a dual-gate configuration where two different layers of unipolar organic semiconductors (OSC) are stacked. In our OFET, the hole-channel for the p-type operation depends primarily on the corresponding gate insulator-OSC interface and the electron-channel for the n-type operation on the remaining interface in an independent manner. Using a combination of two independent gate voltages, the charge transport can be efficiently controlled and the on-off current ratio becomes enhanced in a dual-gate configuration. The optimization of the materials, the interfaces, and the device architectures will lead to a wide range of organic electronic applications.

Keywords ambipolar organic field effect transistors; semiconductor-insulator interfaces; dual gate; solution process; dual interface

1. Introduction

Ambipolar organic field-effect transistors (OFETs) have been extensively studied for understanding the charge transport phenomena [1] and developing organic electronic devices such as light-emitting devices [2] and complementary integrated circuits [3]. An active organic semiconductor (OSC) layer is one of the most critical ingredients in ambipolar OFETs, and generally consists of a single OSC [2, 4] or a blend of two different OSCs [5, 6]. The two cases often encounter with the unbalanced energy barrier and/or high channel resistance from the viewpoints of the charge injection and transport.

Besides the OSC materials themselves, the device architectures using two stacked OSC layers in single gate configuration as shown in Fig. 1(a) have been demonstrated to balance the carrier mobility and to improve the crystalline structure of each OSC layer [7–9]. However, in a single gate configuration, the charge control scheme is still limited. For example, for the current flow from one of two OSCs either in the n-type or the p-type operation, the other OSC acts as an additional insulator or a channel of undesired charge carriers. This leads directly to a low on-off current ratio of an ambipolar OFET.

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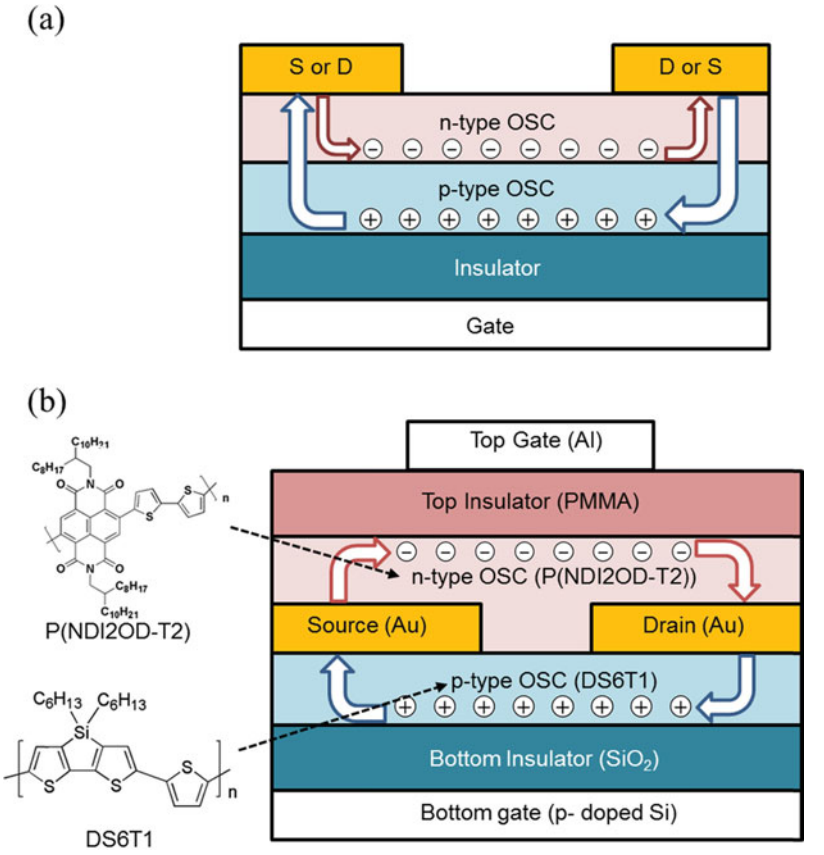

Figure 1. Schematic diagrams of (a) a conventional SI-OFET and (b) our DI-OFET with two active layers of n-type and p-type organic semiconductors (OSCs) together with the chemical structures of the OSCs used. The blue and red arrows represent the charge flow of holes in the p-type OSC and that of electrons in the n-type OSC. The source and the drain are denoted by S and D.

In this work, we present the ambipolar properties of a dual-gate OFET with two OSC-insulator interfaces stacked together. Two active layers of an n-type and a p-type OSCs were stacked between two gate insulator-electrode pairs. In our OFET structure, the bottom gate insulator-bottom OSC interface was involved in the channel for the p-type operation and the top gate insulator-top OSC interface in the channel for the n-type operation. A combination of two gate voltages from two separated, bottom and top electrodes enables to efficiently control the charge carriers for the enhancement of the mobility and the on-off current ratio in the ambipolar operation.

2. Experiment

A schematic diagram of our ambipolar dual-gate OFET is shown in Fig. 1(b). A heavily doped p-type Si substrate was used as a bottom gate electrode and a 300 nm-thick SiO_2 layer was served as the bottom gate insulator. The Si/SiO_2 substrate was cleaned with acetone, isopropyl alcohol, methanol, and deionized water in series for

10 min each under ultra-sonication. The cleaned Si/SiO_2 substrate was subsequently exposed to UV-ozone for 10 min, then spin-coated with hexamethyldisilazane (HMDS) as a buffer layer at 3000 rpm for 30 sec, and finally rinsed to obtain a monolayer of HMDS. A p-type OSC, poly(4,4-di-n-hexyldithienosilole-alt-(bi)thiophene) (DS6T1, P1200) dissolved in dichlorobenzene (DCB) in 1 wt.%, was spin-coated at 2000 rpm for 30 sec, followed by annealing at 70°C for the removal of the solvent and the thickness was measured as 60 nm [10]. The source and drain electrode were prepared with 50-nm-thick gold (Au) which was thermally deposited. Using a shadow mask, the channel length and the channel width were defined to be 150 μm and 1 mm, respectively. An n-type OSC, poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5-(2,29-bithiophene)} [P(NDI2OD-T2), N2200] dissolved in p-xylene in 1 wt.%, was spin-coated at 2000 rpm for 30 sec and subsequently baked at 110°C for 6 hr in a vacuum dry oven. The thickness of N2200 was 60 nm. The top gate insulator was prepared using poly(methyl methacrylate) (PMMA), dissolved in ethyl acetate in 8 wt.%, by spin-coating at 3000 rpm for 30 sec and annealed at 100°C for 1 hr. The thickness of the PMMA film was about 1.8 μm. The top gate electrode was made of 50-nm-thick aluminium (Al). All the electrical characteristics of our ambipolar OFET were measured using a semiconductor analyzer (HP 4155A) at room temperature under ambient condition.

3. Results and Discussion

We first measure the unipolar characteristics of both the n-type and the p-type OSCs in conventional top- and bottom-gate OFETs with single OSC-insulator interfaces (SIs) to optimize the stacking sequence of two OSC-insulator pairs. Figures 2(a)–(d) show the transfer characteristics of the OFETs with P1200 and N2200 in the top- and bottom-gate geometries. The measured mobility of the SI-OFET with P1200 was about 4.7×10^{-4} cm^2/Vs in the top-gate geometry from Fig. 2(a) and 1.3×10^{-3} cm^2/Vs in the bottom-gate geometry from Fig. 2(c). The mobility for the N2200 case was 6.4×10^{-2} cm^2/Vs in the top-gate geometry from Fig. 2(b) and 1.7×10^{-2} cm^2/Vs in the bottom-gate geometry from Fig. 2(d). As a consequence, a bottom-gate geometry for the p-type operation (P1200) and a top-gate geometry for the n-type operation (N2200) are desirable in an ambipolar OFET. This is also hinted by the facts that for the p-type operation, less charge traps are produced at the P1200-SiO_2 interface than the P1200-PMMA interface and N2200 shows the high molecular regioregularity as well as the electronic structure suitable for the n-type operation [11, 12].

Based on the above results, specifically from Figs. 2(b) and 2(c), P1200 and N2200 were used in the bottom-gate and the top-gate geometries, respectively, for constructing an ambipolar-type OFET as depicted in Fig. 1(b). The unipolar and ambipolar electrical characteristics of our OFETs with dual OSC-insulator interfaces (DIs) were investigated under the condition that a single gate voltage was swept (Fig. 3) or two gates were swept (Fig. 4), respectively. First, we discuss the single gate operation of the DI-OFET when one of two gates is floated. For the p-type operation of the DI-OFET when the bottom gate was swept while the top gate was floated, the mobility was measured to be 6.2×10^{-4} cm^2/Vs from Fig. 3(a) and the off-current was substantially increased compared to the SI-OFET case in Fig. 2(c). This is attributed to the formation of a virtual n-channel in the top n-type OSC. Although the hole-channel is turned-off when $V_{GS} = 0$ and $V_{DS} = -80$ V, the electrons would feel as if $V_{GS} = 80$ V and $V_{DS} = 80$ V. In other words, due to the presence of the top n-type OSC, a virtual electron-channel can be formed during the suppression of the hole-channel under the condition that the bottom gate voltage is swept

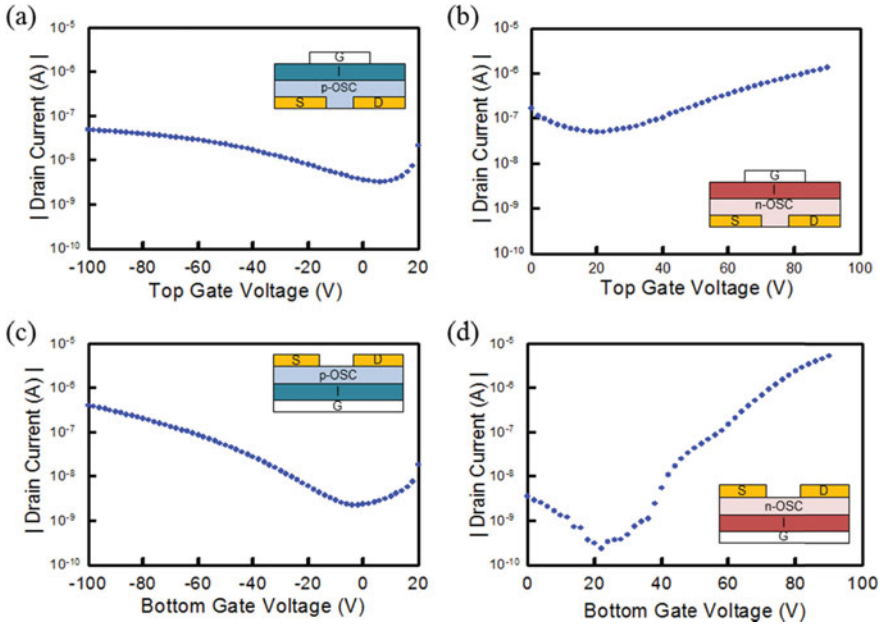

Figure 2. Transfer curves of the SI-OFETs with (a) P1200 and (b) N2200 in the top-gate geometry and the SI-OFETs with (c) P1200 and (d) N2200 in the bottom-gate geometry. The drain voltage for P1200 was −80V and that for N2200 was 80V, respectively. Insets show the corresponding device structures. The source, the drain, the gate, the insulator are denoted by S, D, G, and I, respectively.

toward the negative direction. Consequently, the on-off ratio is decreased due to formation of n-channel in the DI-OFET even in the turn-off voltage region of the p-type SI-OFET. For the n-type operation of the DI-OFET when the top gate was swept while the bottom gate was floated, the mobility was about 5.0×10^{-2} cm^2/Vs, determined from Fig. 3(b),

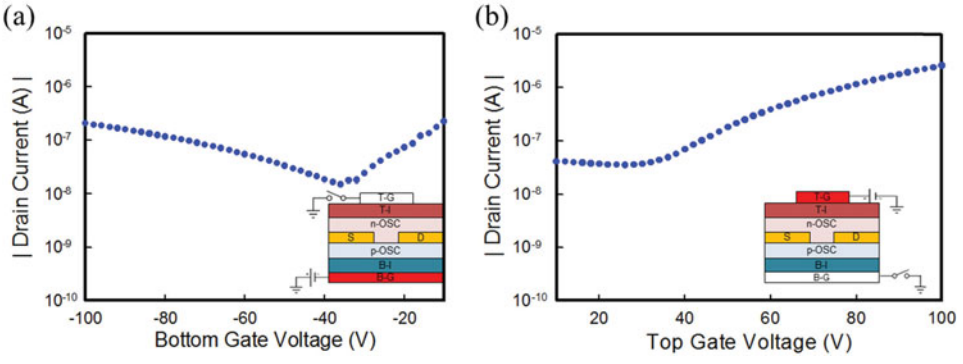

Figure 3. The transfer curves of the DI-OFETs upon sweeping (a) the bottom gate voltage and (b) the top gate voltage under the condition that the counter-gate was floated. The drain voltage for the p-type operation was −80V and that for the n-type operation was 80V, respectively. The bottom gate, the top gate, the bottom insulator, and the top insulator are denoted by B-G, T-G, B-I, and T-I, respectively.

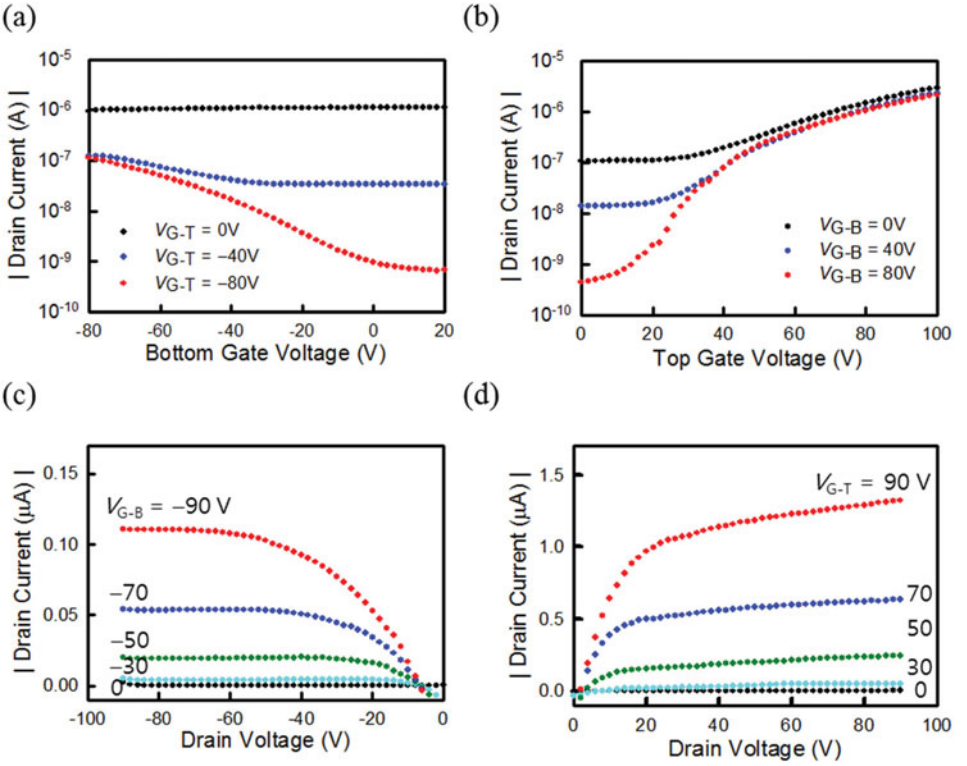

Figure 4. The transfer curves of the DI-OFETs upon sweeping (a) the bottom gate voltage for the p-type operation at the drain voltage of −80V and (b) the top gate voltage for the n-type operation at the drain voltage of 80V. The bias voltages at the top gate and the bottom gate are denoted by $V_{G\text{-}T}$ and $V_{G\text{-}B}$. The output curves of the DI-OFETs as a function of the sweeping drain voltage at several different bias voltages for (c) the p-type operation and (d) the n-type operation. The voltages at the counter-gate electrodes were $V_{G\text{-}T} = 80$ V for the p-type operation and $V_{G\text{-}B} = -80$ V for the n-type operation.

which is slightly decreased from the SI-OFET case in Fig. 2(b). Similar to the formation of electron-channel in the p-type operation in Fig. 3(a), the high off-current and low on-off ratio are observed in this case, which results from the formation of a virtual hole-channel in the bottom p-type OSC layer. This low on-off ratio induced by the formation of virtual counter channel is commonly observed phenomena in ambipolar OFETs, which should be avoided to achieve good electrical properties by means of an electrically controllable scheme such as a dual-gate configuration [13–15].

We now describe the relative roles of the bottom and top gate voltages on the off-current and the output characteristics of our DI-OFETs for the ambipolar-type operation. As shown in Fig. 4(a), for the p-type operation, the off-current as a function of the bottom gate voltage ($V_{G\text{-}B}$) was greatly decreased with increasing a bias voltage at the top gate ($V_{G\text{-}T}$) above a certain value (about −40 V) in the negative direction. It is noted that under zero bias voltage at the top gate ($V_{G\text{-}T} = 0$), the virtual electron-channel is not suppressed at all in our case (black dotted line) irrespective of the bottom gate voltage. The drain current is the sum of the currents in the hole-channel and the electron-channel. Since the drain current flowing in the electron-channel is 10 times greater than that in the hole-channel as shown

in Figs. 2(b) and 2(c), the total drain current does not seem to be modulated by the bottom gate voltage whether the suppression of the hole-channel is occurred or not. For the n-type operation, similar suppression of the off-current was observed with increasing the top gate voltage as shown in Fig. 4(b). The only difference is that the modulation of the drain current is observed even under zero bias voltage at the counter gate ($V_{G\text{-}B} = 0$) compared to the case of Fig. 4(a). This is because even though the virtual hole-channel is formed, the drain current flowing in the hole-channel is much lower than that in the electron-channel.

The on-off current ratio of our ambipolar-type OFET was substantially improved (about one order of magnitude) by the suppression of the virtual-channel but it still remains quite low (only on the order of 10^2). However, it can be much improved by the increase of the on-current through the proper interfacial modification and the optimized channel dimension for given OSC materials. Figures 4(c) and 4(d) show the output characteristics of the DI-OFET as a function of the sweeping drain voltage at several different bias voltages for the p-type operation and the n-type operation, respectively. Clearly, well-behaviors of an ambipolar-like transistor were observed. The saturated drain current in the p-type operation is almost ten times less than that in the n-type operation, which is due to the intrinsic property of the p-type OSC we used. The mobility of the dual-gate DI-OFET was measured to be 5.7×10^{-4} cm^2/Vs for the p-type operation and 6.9×10^{-2} cm^2/Vs for the n-type operation. The dual-gate DI-OFET enables to individually vary the drain current of the p-channel or that of the n-channel, allowing the use of two different OSCs in a stacked manner.

4. Conclusions

We demonstrated a dual-gate configuration of an ambipolar-type OFET with two different OSC-insulator interfaces. The combination of two individual gate voltage is capable of controlling the charge transport in a two stacked organic semiconductors. Our approach may offer one of the solutions to eliminate the disparity of the electrical properties between the p-type operation and the n-type operation in the ambipolar-type OFET. However, the improvement of the device performance through the use of the OSC materials having excellent electrical properties, the precise control of the interfaces, and the optimization of the device architecture remains to be pursued for practical applications as integrated organic circuits.

Acknowledgment

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